



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hisashi Ohtani  
Serial No. : 10/657,137  
Filed : September 9, 2003  
Title : SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION METHOD  
THEREOF

Art Unit : 2811  
Examiner : Unknown  
Confirmation No.: 1909

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Applicant submits the references listed on the attached form PTO-1449.

This statement is being filed before the receipt of a first Office action on the merits.

Please apply any charges or credits to Deposit Account No. 06-1050.

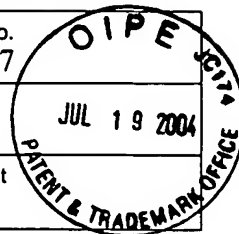
Respectfully submitted,

Date: July 19, 2004

  
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Substitute Form PTO-1449 (Modified)  <b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 07977-152003	Application No. 10/657,137
	Applicant Hisashi Ohtani		
	Filing Date September 9, 2003	Group Art Unit 2811	



U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	6,624,450 B1	09/23/2003	Yamazaki et al.			01/25/1999
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL	06-291314	10/18/1994	JAPAN			Full	
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AQ	
	AR	
	AS	
	AT	

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EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	